

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on November 21, 2003. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

Karen Cinq-Mars 11/21/03
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____:

Chidambarao, Dureseti, et al.:

Serial No. 10/605,108:

Filed: 9/9/03:



November 21, 2003

Group Art Unit: To Be Assigned

Examiner: To Be Assigned

International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: METHOD FOR REDUCED N+ DIFFUSION IN STRAINED SI ON SIGE SUBSTRATE

INFORMATION DISCLOSURE STATEMENT
Under 37 C.F.R. 1.56

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the examiner in charge of the above-identified application.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the examiner and formally made of record in this application.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Dureseti Chidambarao, et al.

By Joseph P. Abate 11-21-03
Joseph P. Abate
Registration No. 30,238
Telephone No. 845-894-4633

FIS920030183US1



FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS920030183US1	SERIAL NO. 10/605,108
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Dureseti Chidambarao, et al.	
(Use several sheets if necessary)	FILING DATE: 9/9/03	GROUP: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
	6,509,618 B2	1/21/03	Jan et al.			
	6,476,462 B2	11/5/2002	Shimizu et al.			
	6,362,082 B1	3/26/2002	Doyle et al.			
	6,228,694 B1	5/8/2001	Doyle et al.			
	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
	6,506,652	01/14/03	Jan, et al.			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

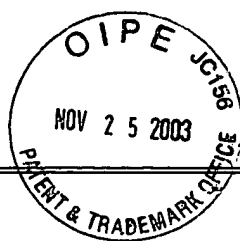
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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DATE CONSIDERED

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	5,081,513	1/14/1992	Jackson, et al.			
	3,602,841	8/31/1971	McGroddy			
	6,531,740	3/11/2003	Bosco, et al.			
	6,531,369	3/11/2003	Ozkan, et al.			
	6,501,121	12/31/2002	Yu, et al.			
	6,498,358	12/24/2002	Lach, et al.			
	6,493,497	12/10/2002	Ramdani, et al.			
	6,403,975	6/11/2002	Brunner, et al.			
	6,361,885	3/26/2002	Chou			
	6,255,169	7/3/2001	Li, et al.			
	6,246,095	6/12/2001	Brady, et al.			
	6,165,383	12/26/2000	Chou			
	6,133,071	10/17/2000	Nagai			
	6,046,464	4/4/2000	Schetzina			
	6,025,280	2/15/2000	Brady, et al.			

FOREIGN PATENT DOCUMENTS

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	5,940,736	8/17/1999	Brady, et al.			
	5,880,040	3/9/1999	Sun, et al.			
	5,861,651	1/19/1999	Brasen, et al.			
	5,679,965	10/21/1997	Schetzina			
	5,670,798	9/23/1997	Schetzina			
	5,561,302	10/1/1996	Candelaria			
	5,471,948	12/5/1995	Burroughes, et al.			
	5,459,346	10/17/1995	Asakawa, et al.			
	5,391,510	2/21/1995	Hsu, et al.			
	5,371,399	12/6/1994	Burroughes, et al.			
	5,108,843	4/28/1992	Ohtaka, et al.			
	5,060,030	10/22/1991	Hoke			
	4,958,213	9/18/1990	Eklund, et al.			
	4,665,415	5/12/1987	Esaki, et al.			

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	5,989,978	11/23/1999	Peidous			
	6,284,626	9/4/2001	Kim			
	6,274,444	8/14/2001	Wang			
	6,261,964	7/17/2001	Wu, et al.			
	6,221,735	4/24/2001	Manley, et al.			
	6,117,722	9/12/2000	Wuu, et al.			
	6,107,143	8/22/2000	Park, et al.			
	6,090,684	7/18/2000	Ishitsuka, et al.			
	6,066,545	5/23/2000	Doshi, et al.			
	6,008,126	12/28/1999	Leedy			
	5,946,559	8/31/1999	Leedy			
	5,840,593	11/24/1998	Leedy			
	5,592,018	1/7/1997	Leedy			
	5,592,007	1/7/1997	Leedy			
	5,571,741	11/5/1996	Leedy			

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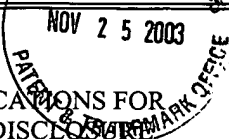
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	5,557,122	9/17/1996	Shrivastava, et al.			
	5,354,695	10/11/1994	Leedy			
	5,134,085	7/28/1992	Gilgen, et al.			
	5,006,913	4/9/1991	Sugahara, et al.			
	4,952,524	8/28/1990	Lee, et al.			
	4,855,245	8/8/1989	Neppl, et al.			

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INFORMATION DISCLOSURE CITATION
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Docket Number (Optional)

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Applicant(s)

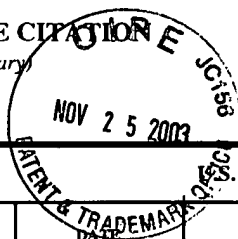
Chidambarrao, Dureseti, et al.

Filing Date

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Group Art Unit

Unassigned



U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Novel Locally Strained Channel Technique for High Performance 55 nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4 IEDM 27
		Local Mechanical-Stress Contro; (LMC): A New Technique for CMOS-Performance Enhancement A. Shimizum. et al. 2001 IEEE, 19.4.1-19.4.4 IEDM 01-433
		Mechanical Stress Effect of Etch-Stop Nitride and its impact on Deep Submicron Design Shinya Ito, et al. 2000 IEEE, 10.7.1-10.7.4 IEDM 00-247
		A Highly Dence, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications F. Ootsuka, et al. 2000 IEEE, 23.5.1-23.5.4 IEDM 00-575

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress Gregory Scott, et al. 1999 IEEE, 34.4.1-24.4.4 IEDM 99-827
		Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4 IEDM 98-707
		Characteristics and Device Design of Sub-100 nm Strained Si N - and PMOSFETs K. Rim, et al. 2002 IEEE, 98-99, 2002 Symposium On VLSI Technology Digest of Technical Papers

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